

as high as that of the output clock, the phase difference of the output clocks is a multiple of  $360/N$  degrees.

21. The method of claim 17 wherein the frequency division is triggered by the first  
5 reference period of the reference clock to generate an output clock, the second  
reference period lagging the first period of the reference clock starting frequency  
division to generate another output clock.
22. The method of claim 17 wherein a third output clock can be produced, output  
10 clock having the same frequency as the two output clocks but different phase, the  
method further comprising:  
generating a second reference clock having the same clock frequency but a  
different reference phase as the reference clock; and  
triggering each period of the third output clock according to each period of  
15 the second reference clock.

#### Abstract of Disclosure

The invention relates to a method and related circuitry for multiple  
20 phase-splitting. The method includes: while generating  $M$  output clocks  
with a same frequency  $f_1$  and different phases, generating  $N$  reference  
clocks with a same frequency  $(M/N)*f_1$  and different phases (wherein  
 $M > N$ ), and triggering  $(N/M)$  frequency division using different periods  
within each reference clock to generate  $(M/N)$  output clocks of different  
25 phases for each reference clock, such that the  $M$  output clocks of  
different phases are generated from the  $N$  reference clocks of different  
phases.

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